UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/038,501	01/03/2002	Robert C. Sundahl	5038-151	5497

32231 7590 02/08/2006

MARGER JOHNSON & MCCOLLOM, P.C.
210 SW MORRISON STREET, SUITE 400
PORTLAND, OR 97204

EXAMINER	
NGUYEN, KEVIN M	

ART UNIT	PAPER NUMBER
2674	

DATE MAILED: 02/08/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/038,501	SUNDAHL ET AL.	
	Examiner	Art Unit	
	Kevin M. Nguyen	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 December 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *03 January 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Request for Continued Examination

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 12/09/2005 has been entered. An action on the RCE follows:

2. This office action is made in response to applicant's amendment/argument filed on 12/09/2005. Claims 25-30 are cancelled, and claims 1, 14 and 18 are amended. Thus, claims 1-24 are currently pending in the application. Applicant's arguments, see pages 6, with respect to amended claims 1, 14 and 18 are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-24 are rejected under 35 U.S.C. 102(b) as being anticipated by Ju et al (US 5,497,258) hereinafter Ju.

5. It is respectfully submitted that in the case law stated "Drawing as a Reference", "Things clearly shown in reference patent drawing qualify as prior art features, even though unexplained by the specification". See In re Mraz, 173 USPQ 25 (CCPA 1972). "A claimed invention may be anticipated or rendered obvious by a drawing in a reference, whether the drawing disclosure by accidental or intentional. However, a drawing is only available as a reference for what it would teach one skilled in the art who did not have the benefit of applicant's disclosure". See In re Meng, 181 USPQ 94, 97 (CCPA 1974). "Absent of any written description in the reference specification of quantitative values, arguments based on measurement of a drawing are of little value in proving anticipation of a particular length". See In re Wright, 193 USPQ 332, 335 (CCPA 1977).

6. As to claim 1, Figure 1 of Ju teaches a device for rendering an image, comprising:

an integral panel [a liquid crystal spatial light modulators (SLMs) panel 10 are integrated circuit into a single device, see col. 1, lines 18-22] having a viewing side [a cover glass 13, see Fig. 1, see col. 4, lines 27-30] that includes a front panel surface [an antireflective coating 28, see Fig. 1, col. 4, lines 29] and a non-viewing side [a substrate 11, see Fig. 1, col. 8, lines 52-55] that includes a rear panel surface opposed to and facing away from the front panel surface, said non-viewing side having:

Figure 5 of Ju further teaches a peripheral region formed on the rear panel surface [pads 37, solder joints 27, and four-sided wire bond path 19 are on the substrate 11, see col. 8, lines 12-15];

Figure 5 of Ju further teaches a central region formed on the rear panel surface [VLSI chip 12, see col. 8, lines 15-25];

Figures 1 and 5 of Ju further teach a pattern of contacts [solder pads 25, 26 36 of VLSI chip 12] exposed to the rear panel surface formed in the central region of the non-viewing side [see col. 8, lines 46-59].

As to claim 2, Ju teaches wherein the pattern of contacts is configured to receive a component [the solder pads 25, 26, 36 of VLSI chip 12, see Figs. 1 and 5, wires or wire bonds 19 are provided on all four sides of VLSI chip 12 to connect the individual pixel circuits of chip 12 to the circuit path that are carried by substrate 11, see col. 4, lines 62-65].

As to claim 3, Ju teaches wherein the component is a printed circuit board [the substrate member 11 is a silicon wafer having a plated wire pattern on the upper surface thereof, see col. 4, lines 22-24].

As to claim 4, Ju teaches wherein the component is an integrated circuit [the Very Large Scale Integration (VLSI) chip 12, see Fig. 5, the abstract, and the title].

As to claim 5, Ju teaches wherein the component is a view device driver circuit [a driver D drives the VLSI's metal crystal modulating pad, LC pad 45 of Fig. 7, see col. 7, lines 32-38].

As to claim 6, Ju teaches further comprising a socket coupled to the pattern of contacts and structured to receive a component in the central zone [the VLSI chip 12 inherent has a plurality of pins that receives into which the substrate 11 can be inserted, see Fig. 1, and the abstract, lines 5-10].

As to claim 7, Fig. 5 of Ju teaches wherein the pattern of contacts is configured to receive a plurality of components in the central zone [the VLSI 12 has the pattern of contacts corresponding to the solder pads 25, 26, 36 in the central zone, see Fig. 5].

As to claim 8, Fig. 5 of Ju teaches further comprising a plurality of components connected to the non-viewing side of the panel [two or more VLSI chip 12 are accurately located relative to a single underlying substrate member 11, see col. 9, lines 35-38].

As to claim 9, Ju teaches further comprising a display contact layer [the LD pads 45 also act a pixel reflectors for the liquid crystal layer, see col. 7, lines 45-46], a dielectric layer [the glass 13, see col. 8, line 64], and an electrically conductive circuit layer including the pattern of contacts [the VLSI 12 has the pattern of contacts corresponding to the solder pads 25, 26, 36, see Fig. 5].

As to claim 10, Ju teaches wherein the display contact layer couples the plurality of display cells and the electrically conductive circuit layer [the LD pads 45 also act a pixel reflectors for the liquid crystal layer, the VLSI 12 has the pattern of contacts corresponding to the solder pads 25, 26, 36 that contacts the LD pads 45 , see col. 7, lines 50-53].

7. As to claim 11, Ju teaches wherein the electrically conductive circuit layer couples the display contact layer and the bond pad [FIG. 7 is a top view of VLSI chip 12 in FIG. 1, showing the pixel arrangement of LC pads 45 to each of which a circuit of FIG. 3 is connected, see col. 7, lines 50-53].

As to claim 12, Ju teaches wherein the bond pad layer includes a plurality of bond pads operative to couple the electrically conductive circuit layer to an attached

component [the LD pads 45 also act a pixel reflectors for the liquid crystal layer, the VLSI 12 has the pattern of contacts corresponding to the solder pads 25, 26, 36 that contacts the LD pads 45 , see col. 7, lines 50-53].

As to claim 13, Ju teaches wherein the bond pad layer includes a plurality of bond pads operative to couple the electrically conductive circuit layer to an attached plurality of components [the LD pads 45 also act a pixel reflectors for the liquid crystal layer, the VLSI 12 has the pattern of contacts corresponding to the solder pads 25, 26, 36 that contacts the LD pads 45 , see col. 7, lines 50-53; two or more VLSI chip 12 are accurately located relative to a single underlying substrate member 11, see col. 9, lines 35-38].

8. As to claim 14, Ju teaches a viewing device, comprising:

a panel [a spatial light modulators (SLMs) panel 10, see Fig. 1] including:

a plurality of display cells [a plurality of pixels, see Fig. 3, col. 7, lines 17-22] distributed on the first side of the panel [a cover glass 13, see Fig. 1], the display cells [the plurality of pixels] configured to display an image [a visual image, see col. 2, lines 61-65] that is viewable on a front panel surface formed on the first panel side [the cover glass 13];

a rear surface [a substrate member 11, see Fig. 1] opposed to a facing away from the front panel surface, the rear panel surface formed on a second side of the panel;

a central zone [element 12, see Fig. 5] and a peripheral zone [elements 37/27, see Fig. 5] formed on the rear panel surface [the substrate member 11, see fig. 1];

a matrix of interconnects exposed to the rear panel surface, the matrix of interconnects structured to connect a component to the rear panel surface in the central zone [the solder pads 25, 26, 36 of VLSI chip 12, see Figs. 1 and 5, wires or wire bonds 19 are provided on all four sides of VLSI chip 12 to connect the individual pixel circuits of chip 12 to the circuit path that are carried by substrate 11, see col. 4, lines 62-65].

9. Claim 15 shares the same limitations as those of claim 13 and therefore the rationale for rejection will be the same.

10. Claim 16 shares the same limitations as those of claim 13 and therefore the rationale for rejection will be the same.

11. Claim 17 shares the same limitations as those of claim 6 and therefore the rationale for rejection will be the same.

12. As to claim 18, Ju teaches an electronic display system, comprising:

an image generator [the voltage on the data line is passed to the input capacitance of driver D, see Fig. 3, col. 7, lines 35-37];

a display interface coupled to the image generator [the driver D drives, or charges, the VLSI's metal crystal modulating LC pad 45 of Fig. 7, see col. 7, lines 37-38];

a display coupled to the display interface [LC pads, see col. 7, lines 50-53], the display including:

a panel [the SLMs panel 10, fig. 1] having a first side [a cover glass 13] and a second side [a substrate 11], the first side of the panel including a plurality of display cells distributed thereon [a plurality of pixels, see col. 7, line 22], the plurality of display cells structured to display an image [a visual image, see col. 2, line 62] that is viewable from the first side of the panel, the second side of the panel being opposed to and facing away from the first side of the panel [the substrate 11, see Fig. 1];

a matrix of interconnects exposed to a surface formed on the second side of the panel, the matrix of interconnects structured to connect a component to the second side of panel [the solder pads 25, 26, 36 of VLSI chip 12, see Figs. 1 and 5, wires or wire bonds 19 are provided on all four sides of VLSI chip 12 to connect the individual pixel circuits of chip 12 to the circuit path that are carried by substrate 11, see col. 4, lines 62-65].

13. As to claim 19, Fig. 5 of Ju teaches wherein the panel further includes a periphery and the component is connected to the panel within the periphery [pads 37, solder joints 27, and four-sided wire bond path 19 are on the substrate 11, see col. 8, lines 12-15].

14. As to claim 20, Fig. 5 of Ju teaches wherein a plurality of components are connected to the panel within the periphery [pads 37, solder joints 27, and four-sided wire bond path 19 are on the substrate 11, see col. 8, lines 12-15].

15. Claim 21 shares the same limitations as those of claim 3 and therefore the rationale for rejection will be the same.

16. Claim 22 shares the same limitations as those of claim 4 and therefore the rationale for rejection will be the same.

17. Claim 23 shares the same limitations as those of claim 6 and therefore the rationale for rejection will be the same.

18. As to claim 24, Fig. 1 of Ju teaches further comprising a video driver [the drive D, the VLSI chip 12] interposed between the display interface [LC layer 16] and the matrix of interconnects [pads 37, solder joints 27, and four-sided wire bond path 19].

Response to Arguments

19. Applicant's arguments with respect to claims 1-24 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

20. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kevin M. Nguyen whose telephone number is 571-272-7697. The examiner can normally be reached on MON-THU from 8:00-6:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, Patrick N. Edouard who is a supervisor Division 2629 can be reached on 571-272-7603. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8000.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for

published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the Patent Application Information Retrieval system, see http://portal.uspto.gov/external/portal/pair. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Kevin M. Nguyen
Patent Examiner
Division 2629

KMN
February 2, 2006